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Express Mail No. EM502298395US

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor(s): Paul Michael Embree And Jeffrey Mark Claar

For: MEMORY ALLOCATION FOR REAL-TIME AUDIO PROCESSING

Enclosed are:

- ☒ 6 sheets of Formal Drawing(s) including 6 figures.
- ☒ An Assignment of the invention to: SONY CORPORATION AND SONY PICTURES ENTERTAINMENT, INC.
- ☒ A Declaration and Power of Attorney.
- ☐ A Verified Statement to establish Small Entity Status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ _____

The Filing Fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
For:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
Basic Fee:	-	-	-	$385.00	-	$770.00
Total Claims:	9	0	$11.00	$0.00	$22.00	$0.00
Indep. Claims:	2	0	$40.00	$0.00	$80.00	$0.00
☐ Multiple Dep. Claim(s) Presented			$130.00	$0.00	$260.00	$0.00
*If the difference in (Col. 1) is less than zero, enter "0" in (Col. 2)			Total:	$0.00	Total:	$770.00

- ☒ A check in the amount of $770.00 to cover the filing fee is enclosed.
- ☒ A check for $40.00 covering Recordation of Assignment is enclosed, along with the Assignment Cover Sheet.
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  - ☒ Any additional filing fees required under 37 CFR 1.16.
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☒ Any extension or petition fees under 37 CFR §1.17.

☒ Any filing fees under 37 CFR §1.16 for presentation of extra claims.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: September 24, 1997

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Our Ref. No. 080398.P115
Express Mail No.: EM502298395US

UNITED STATES PATENT APPLICATION

FOR

MEMORY ALLOCATION FOR REAL-TIME AUDIO PROCESSING

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to memory allocation for real-time audio processing. In particular, the present invention relates to DRAM bank switching for real-time audio data storage.

2. Description of Related Art

Real-time audio signal processing requires fast access time. In a typical audio system, there are general-purpose processor and specialized digital signal processor (DSP). The general purpose or host processor is any general central processing unit (CPU) such as those in a personal computer (PC). The host processor usually performs data storage, user interface, network control, and other general command and house keeping functions. The host processor also has interfaces to peripheral devices such as serial communication, disk controllers (e.g., a hard disk controller). The DSP usually performs signal processing functions to process real-time audio data such as digital filtering. Multiple and separate memory banks are accessible to both the host processor or other direct memory access (DMA) devices such as a SCSI controller.

Real-time audio signal processing usually involves three basic operational modes: recording, playback, and editing.

During the recording mode, the audio data are sent from audio input channels and stored in random access memories (RAMs) by the DSP. The

audio data are subsequently transferred to a storage device such as a hard disk drive via the SCSI controller.

During the playback mode, the audio data stored in the hard disk drive are first transferred to random access memory (RAM) via the SCSI controller. The DSP then accesses the RAM to process the audio data and output to the appropriate audio output channels.

The RAM is typically organized as multiple memory banks which are accessible to both the DSP and the SCSI controller. Traditional techniques involve transferring data to fill up a memory bank before going to the next memory bank. However, if a memory bank is busy for receiving data, it will not be immediately accessible to the DSP, resulting in processing delay.

Accordingly, there is a need to provide an apparatus and method for efficient memory allocation for real-time audio signal processing.

SUMMARY OF THE INVENTION

The present invention discloses a method for allocating real-time audio data from N audio channels in a system having a first processor and a second processor. The method comprises the steps of: (1) providing P memory banks where each memory bank is accessible to the first and second processors; and (2) storing P subsets of the audio data in P memory banks, respectively, where the P subsets correspond to P different groups of audio channels.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which:

Figure 1 is a block diagram illustrating one embodiment of an audio player/recorder system that operates in accordance with the teachings of the present invention.

Figure 2 is a diagram illustrating one embodiment of an embedded box in the audio player/recorder system.

Figure 3 is a diagram illustrating one embodiment of memory banks.

Figure 4 is a timing diagram illustrating the sampling of an audio signal.

Figure 5 is a diagram illustrating one embodiment of the allocation of sampled audio data stored in the memory banks.

Figure 6 is a flowchart of one embodiment of a process for reading and playing back of audio data in accordance with the principles of the present invention.

DESCRIPTION OF THE PRESENT INVENTION

The present invention discloses a method for efficient memory allocation to reduce memory waiting time in a real-time audio signal processing system. The memory is divided into separate memory banks for independent accesses by the host processor and the digital signal processor (DSP). The audio samples are stored in the memory banks in an interleaving manner to distribute the memory access over multiple memory banks. This memory allocation allows a small computer system interface (SCSI) controller and the DSP equal access to the memory banks.

In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well known electrical structures and circuits are shown in block diagram form in order not to obscure the present invention unnecessarily.

Referring to Figure 1, a block diagram illustrating one embodiment of an audio player/recorder system 100 that operates in accordance with the teachings of the present invention is shown. The system 100 comprises embedded boxes (EBX) EBX1 through EBXN 110_1 through 110_N ("N" being a whole positive number), K remote client computers (RCCs) 120_1 through 120_K ("K" being a positive whole number), network channel 115, audio engineering society (AES) standard input/output channels 125, and synchronizing clock 130.

Each of the EBX 110_1 through 110_N is an audio signal processing system with mass storage. In one embodiment, each EBX includes a personal computer (PC) system and one or more digital signal processors (DSPs). Other configurations that provide similar functionalities are also contemplated. Audio sampled data are stored in multiple dynamic random access memory (DRAM) banks. These DRAM banks are accessible to both the host processor of the PC and the DSPs. The details of the EBX architecture will be discussed later.

Each of the RCC's 120_1 through 120_K provides graphical user interface (GUI) to users for sending command and control information to the EBXes 110_1 through 110_N over the network channel 115. Each RCC has two modes of communication with the EBXes: individual addressing and broadcasting. In individual addressing, the RCC issues the command/control information to the specified EBX. The individual address of the destination is encoded as part of the command/control information.

The AES I/O channels 125 consist of 16 audio I/O channels per EBX conforming to the AES standard. The standard is AES 3-1992 and is available from the Audio Engineering Society, Inc., located in New York, New York. The synchronizing clock 130 provides a master timing signal for synchronizing all real-time activities of the EBXes 110_1 through 110_N.

Referring to Figure 2, a block diagram illustrating one embodiment of the EBX 110 is shown. The EBX 110 comprises one or more processors 205_1 - 205_M ("M" being a positive whole number) and a main memory element 230 (e.g., dynamic random access memory "DRAM", static random access memory "SRAM" etc.) coupled together by a chipset 220. In general, the

chipset 220 operates as an interface between a host bus 210 and a peripheral bus 235.

Processors 205_1 - 205_M are any microprocessors. In this embodiment, processors 205_1 - 205_N are the Pentium® or Pentium Pro® microprocessors manufactured by Intel Corporation at Santa Clara, California.

Chipset 220 typically includes cache DRAM controller (CDC), peripheral bus controller, and data path unit (DPU). The Peripheral Component Interconnect (PCI) Bridge (PB) provides a set of host-to-PCI and PCI-to-host bus transaction translations.

The host bus 210 is a bus that can support transactions to a number of connected processors. Host bus 210 may be referred to as a parallel bus or multiprocessor bus because it supports parallel operations and multiple processors. It is contemplated that host bus 210 operates in a pipelined manner to increase efficiency. However, these features should not be construed to limit the teachings of the present invention. The present invention can be utilized even if there is only one processor connected to the host bus 210, or the host bus 210 is a uniprocessor bus.

The peripheral bus 235 provides a communication path between the processors 205_1-205_M or main memory element 230 and a plurality of peripheral devices 250_1-250_P ("P" being a positive whole number). These peripheral devices 250_1-250_P may include I/O devices such as disk controller 250_1, local area network (LAN) card 250_2. In one embodiment, the disk controller 250_1 is a small computer system interface (SCSI)-2 controller which is interfaced to a number of mass storage devices such as optical read/write drive 252 and hard drive 254, through the SCSI-2 bus. Relevant to the present

invention is the signal processing subsystem (SPS) 270 which includes digital signal processors (DSPs), multiple dynamic random access memory (DRAM) banks and PCI bus interface circuits. The SPS 270 has interface to the serial input/output communication device 272 which is connected to the AES I/O channel interface 274. The peripheral bus 235 may include a Peripheral Component Interconnect (PCI) bus or any other type of bus architecture.

The expansion bus 255 provides a communication path between the peripheral bus 235 and a plurality of expansion peripheral devices 260_1-260_L ("L" being a positive whole number). The expansion bus 255 may include an Industry Standard Architecture (ISA) bus or an Extended Industry Standard Architecture (EISA) bus.

The PCI-to-ISA/EISA Bridge 240 provides the communication path between the peripheral or PCI bus 235 and the expansion or ISA/EISA bus 255.

The term PCI processor refers to a processor that can have control of the PCI bus for data transfers. A # symbol after a signal name indicates an active LOW signal. The absence of such symbol indicates an active HIGH signal. The notation 0x refers to a hexadecimal notation.

The SPS 270 includes one or more digital signal processors (DSPs) and a number of memory banks. The SPS 270 includes a memory system 300 that operates in accordance with the teachings of the present invention.

Referring to Figure 3, a block diagram illustrating one embodiment of the memory system 300 is shown. Memory system 300 comprises two 2-to-1 multiplexers MUX0 310 and MUX1 311 and two memory banks DRAM

BANK0 and DRAM BANK1 320 and 321. As will be explained later, a system having N memory banks can be used with N 2-to-1 multiplexers.

MUX0 310 and MUX1 311 are 2-to-1 multiplexers connected to the DSP bus and the PCI bus (for SCSI access) and to the DRAM BANK0 320 and DRAM BANK1, respectively. Each of the MUX0 310 and MUX1 311 conceptually consists of two multiplexers: address multiplexer (unidirectional) and data multiplexer (bi-directional). For clarity, only one multiplexer is shown and the direction is shown to be bi-directional. In the present embodiment, the multiplexers are realized by the bi-directional switches Part No. QS3257 or similar devices manufactured by Quality Semiconductor (Santa Clara, California).

MUX0 310 and MUX1 311 are controlled by the SEL0 and SEL1 signals, respectively. When SEL0 and SEL1 are at a first logic level (e.g., LOW), the data transfer is between the selected DRAM bank and the PCI bus (SCSI controller). When SEL0 and SEL1 are at a second logic level (e.g., HIGH), the data transfer is between the selected DRAM bank and the DSP bus.

DRAM BANK0 320 and DRAM BANK1 321 are two dynamic random access memory (DRAM) banks operating separately and independently. As is well known by one skilled in the art, other types of memory such as static RAM can also be used. In one embodiment, each DRAM bank is organized as 4Mx32 or 16 Mbytes.

By controlling the SEL0 and SEL1, the two DRAM banks can be accessed simultaneously by two different processors. For example, the SCSI controller may access DRAM BANK0 320 for storing data while the DSP is reading the data out from DRAM BANK1 321.

Referring to Figure 4, a timing diagram 400 illustrating the sampling of audio signals is shown. Timing diagram 400 consists of audio clock 410, clock (CLK) 420, and audio sampled data 430.

Audio clock 410 is a clock that correspond to the audio sampling rate of 48 KHz which results in a sampling period of approximately 20 microseconds. In one embodiment, during each sampling period, 16 samples from 16 audio channels are received from the serial AES input ports and stored in the DRAM banks in recording mode. During the same sample period, the playback of the digital audio is done by reading the data stored in the DRAM banks and sending it to the serial AES output ports.

CLK 420 indicates the separation of 16 channels during each audio clock period. Audio sampled data 430 show the series of sampled audio data. Each of the sampled data corresponds to an audio sample at each channel. The number of samples obtained at each time interval depends on the number of selected channels. In one embodiment, the number of selected channels is 16. For the embodiment shown in Figure 4, during time interval T1, 16 samples from 16 channels, one from each channel, are obtained. Thereafter, the next 16 samples from 16 channels obtained during time interval T2.

Referring to Figure 5, a diagram showing the allocation of audio sampled data in the two memory banks is shown. DRAM BANK 0 is configured to store audio sampled data from channels 0, 2, 4, . . . 14 (the even channels). DRAM BANK 1 is configured to store audio sampled data from channels 1, 3, 5, . . . 15 (the odd channels).

This allocation scheme can be extended to more than two memory banks. The objective is to distribute equally the storage of all audio channels

over the entire memory banks so that the access of all 16 channels is not concentrated into one or a few memory banks. With this equal allocation, there is less chance for the SCSI controller and the DSP to access to the same memory bank at the same time. Even when they do, one processor does not have to wait for too long for its turn to access memory. The result is that audio sampled data are written into or read out of the memory banks at a faster rate to accommodate real-time processing.

For example, if there are P memory banks, DRAM BANK0 will store sampled data from channel 0, channel P, channel 2P, channel 3P, etc. DRAM BANK1 will store sampled data from channel 1, channel P+1, channel 2P+1, channel 3P+1, etc. DRAM BANKP will store sampled data from channel P-1, channel 2P-1, channel 3P-1, etc. In general, each DRAM bank should store a subset of audio data which corresponds to a different group of audio channels.

Referring to Figure 6, a flowchart showing the process S600 to read the audio samples from mass storage and playback the audio data, is shown. In this embodiment, two memory banks (DRAM BANK0 and DRAM BANK1) are used. Recording is accomplished using the same memory allocation method.

Proceeding from a START state, the process S600 enters step S610. In step S610, the host processor determines the location of the audio data which will be used to instruct the SCSI controller to read the audio sampled data from the hard disk or other mass storage devices. The process S600 next enters the decision step S620 to determine whether the channel number is even or odd. If it is determined that the channel number is even, the process S600 enters the step S630 to select and allocate a block of memory in the

DRAM BANK0 for storing the sampled data. Thereafter, the process S600 enters the step S640 to write the audio sampled data into the DRAM BANK0. The process is then terminated.

If it is determined that the channel number is odd, the process S600 enters the step S631 to select the DRAM BANK1 for storing the sampled data. Then in step S641, the audio sampled data is written into DRAM BANK1. The process is then terminated.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

What is claimed is:

1. A method for allocating real-time audio data from N audio channels in a system having a first processor and a second processor, the method comprising the steps of:

providing P memory banks, each memory bank being accessible to the first and second processors; and

storing P subsets of said audio data in P memory banks, respectively, P subsets corresponding to P different groups of audio channels.

2. The method of claim 1, prior to the step of storing, further comprises a step of selecting said memory banks for access by one of the first and second processors.

3. The method of claim 1 wherein P is equal to two.

4. The method of claim 3 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

5. A system having first and second buses for processing real-time audio data from N audio channels, the system comprising:

a first processor and a second processor coupled to said first and second buses, respectively; and

P memory banks coupled to said first and second buses for storing said audio data, said P memory banks being accessible to said first and second processors, said P memory banks storing P subsets of said audio data, respectively, said P subsets corresponding to P different groups of audio channels.

6. The system of claim 5 further comprises P selectors coupled said first and second buses to select said memory banks for access by one of said first and second processors.

7. The system of claim 6 wherein P selectors include P address multiplexers and P data transceivers.

8. The system of claim 5 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

9. The system of claims 5, wherein the P memory banks include dynamic random access memories.

ABSTRACT OF THE DISCLOSURE

The present invention discloses a method for allocating real-time audio data from N audio channels in a system having a first processor and a second processor. The method comprises the steps of: (1) providing P memory banks where each memory bank is accessible to the first and second processors; and (2) storing P subsets of the audio data in P memory banks, respectively, where the P subsets correspond to P different groups of audio channels.

Our Docket No.: 080398.P115

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

MEMORY ALLOCATION FOR REAL-TIME AUDIO PROCESSING

the specification of which

__X__ is attached hereto.
_____ was filed on _____ as
Application No. _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing

date of this application:

APPLICATION NO.	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Rober A. Diehl, Reg. No. P40,992; Tarek Fahmi, Reg. No. P41,402; Karen L. Feisthamel, Reg. No. 40,264; James Y. Go, Reg. No. P40,621; Tarek N. Fahmi, Reg. No. P41,402; David R. Halvorson, Reg. No. 33,395; Eric Ho, Reg. No. 39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Robert Andrew Diehl, Reg. No. P40,992; Sharmini Nathan Green, Reg. No. P-41,410; Thomas A. Hassing, Reg. No. 36,159; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Paul Michael Embree Date 9/24/97

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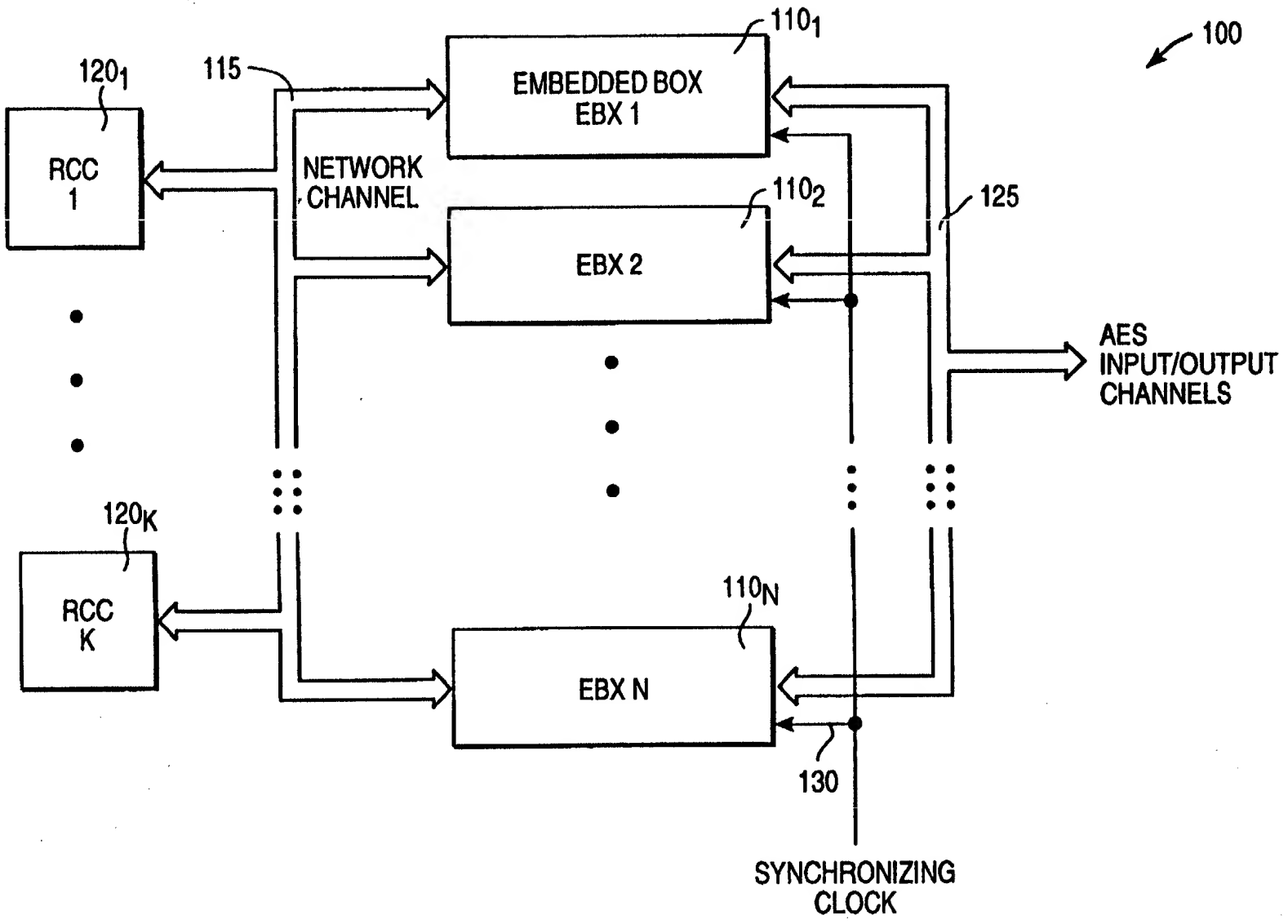
Inventor's Signature Jeffrey Mark Claar Date 9/24/97

Residence ALISO VIEJO, CALIFORNIA (City, State) Citizenship U.S.A. (Country)

Post Office Address 23411 SUMMERFIELD, #39B

ALISO VIEJO, CALIFORNIA 92656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110_1
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120_1
115
RCC
1
NETWORK
CHANNEL
110_2
125
EBX 2
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CHANNELS
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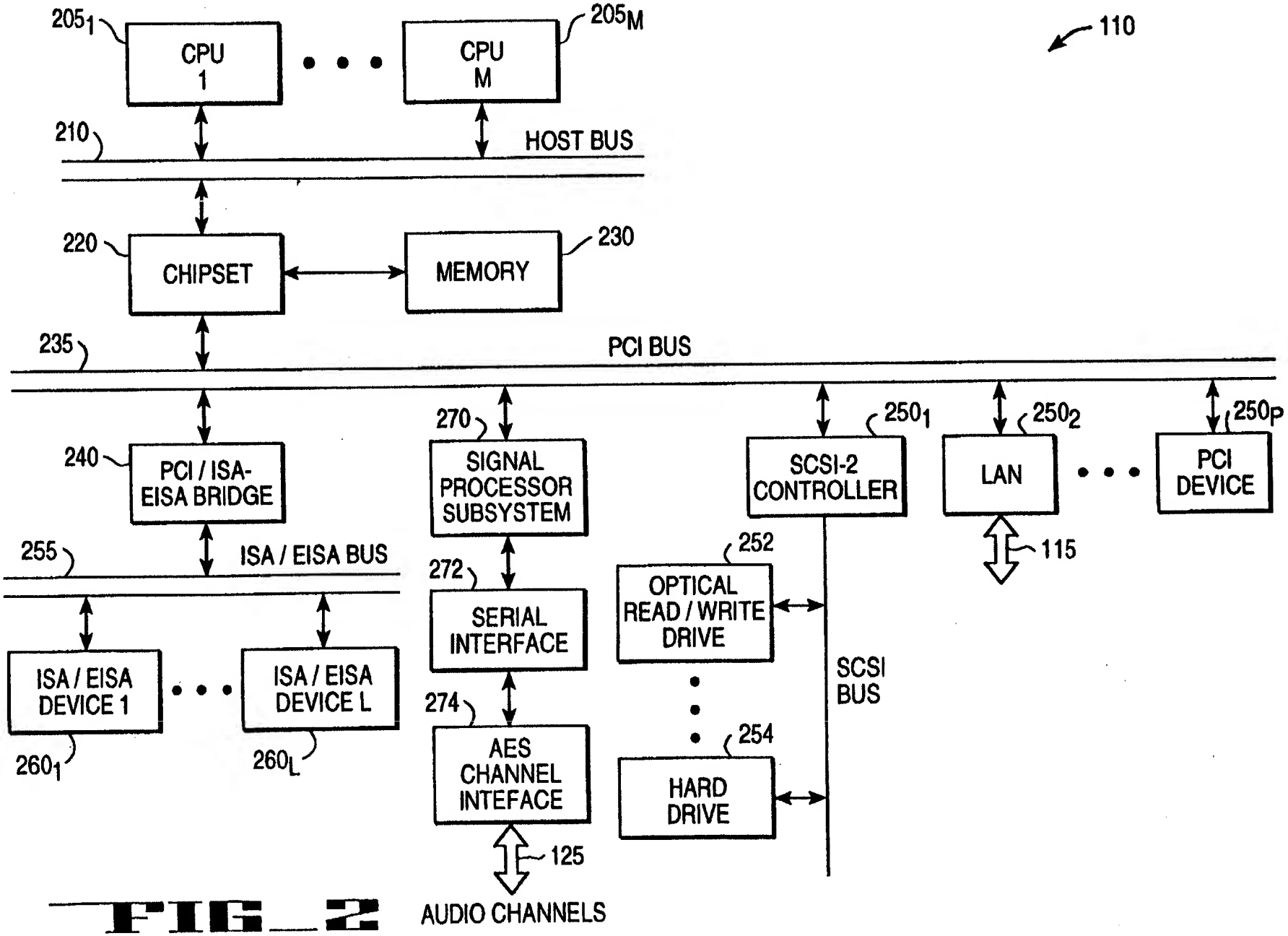
110_N
EBX N
130
SYNCHRONIZING
CLOCK

FIG_1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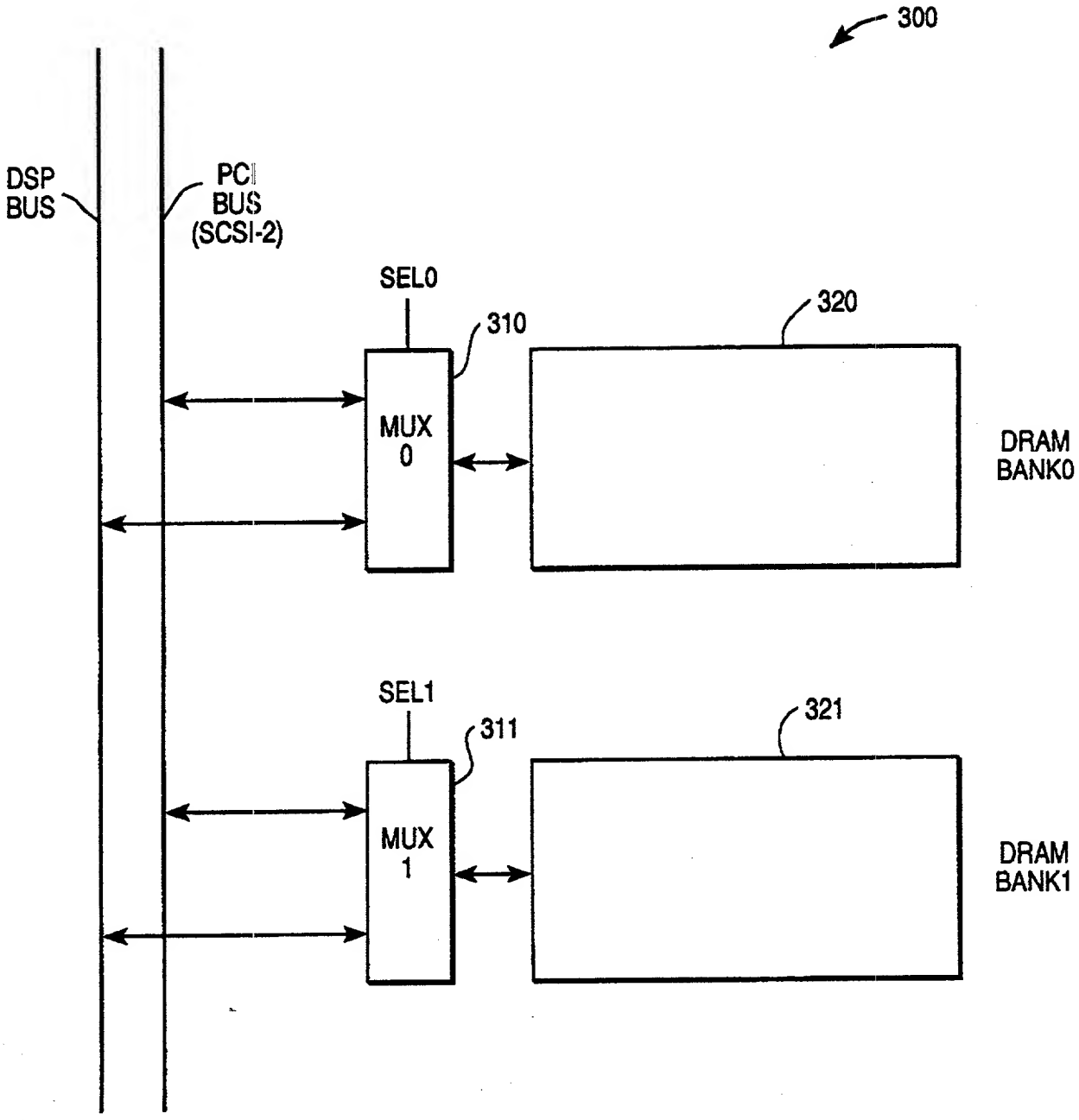
CPU 1
205_M
CPU M
110
210
HOST BUS
220
CHIPSET
MEMORY
230
235
PCI BUS
240
PCI / ISA-EISA BRIDGE
270
SIGNAL PROCESSOR SUBSYSTEM
250_1
SCSI-2 CONTROLLER
250_2
LAN
250_P
PCI DEVICE
255
ISA / EISA BUS
272
SERIAL INTERFACE
252
OPTICAL READ / WRITE DRIVE
115
ISA / EISA DEVICE 1
ISA / EISA DEVICE L
260_1
260_L
274
AES CHANNEL INTEFACE
254
HARD DRIVE
SCSI BUS
125
AUDIO CHANNELS

FIG_2


300
DSP
BUS
PCI
BUS
(SCSI-2)
SEL0
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320
MUX
0
DRAM
BANK0
SEL1
311
321
MUX
1
DRAM
BANK1

FIG_3

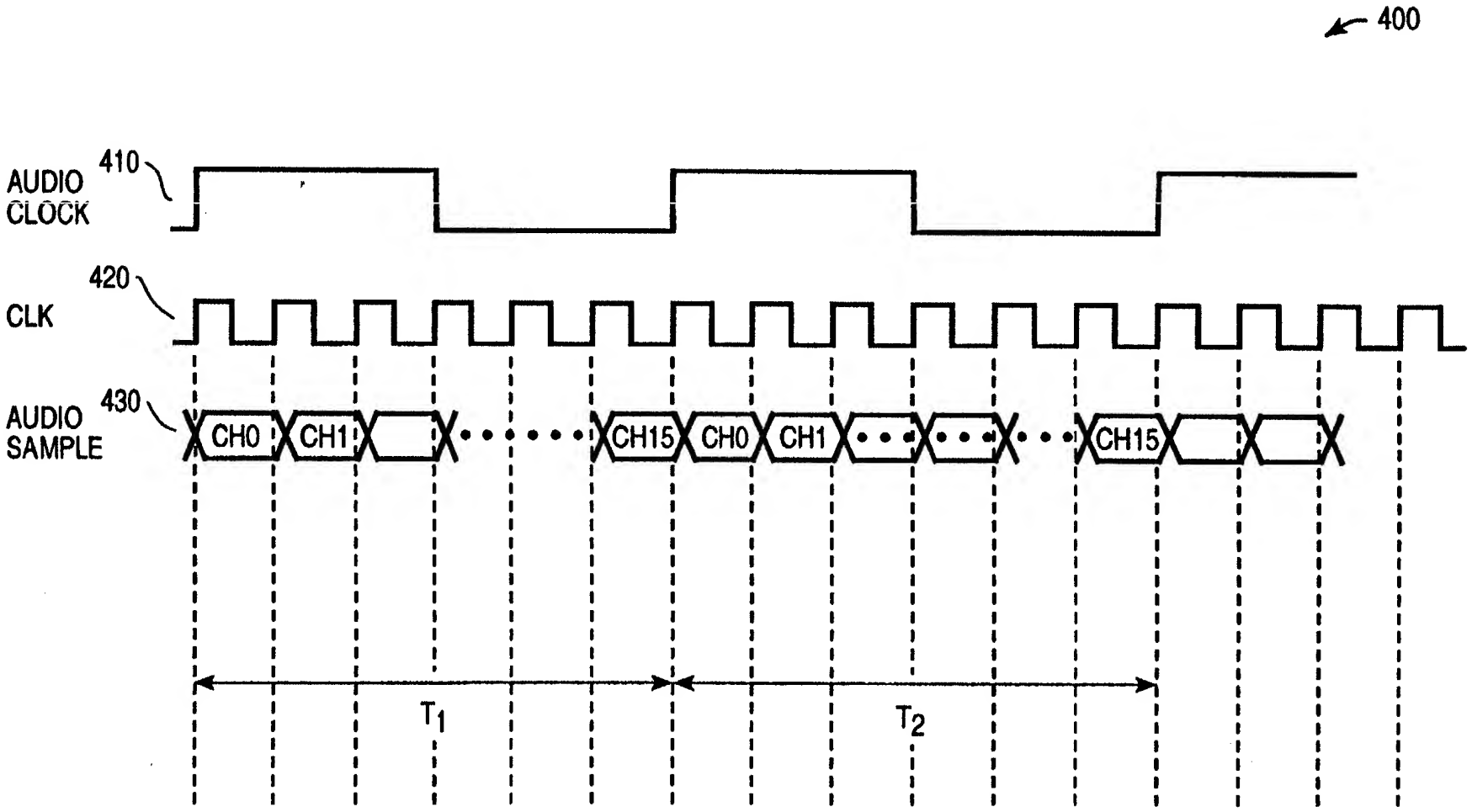
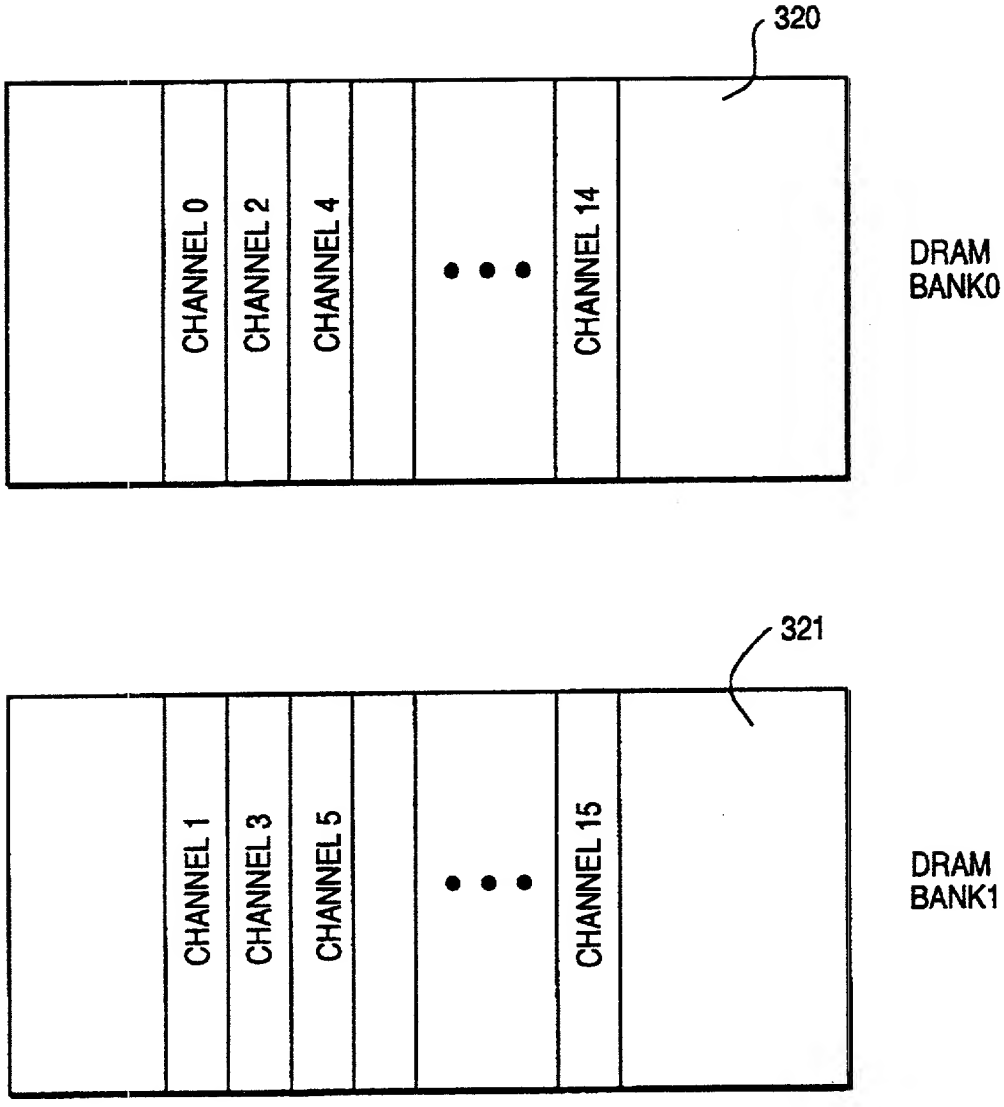

400
410
AUDIO CLOCK
420
CLK
430
AUDIO SAMPLE
CH0
CH1
CH15
CH0
CH1
CH15
T1
T2

FIG_4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CHANNEL 2
CHANNEL 4
CHANNEL 14
DRAM BANK0
321
CHANNEL 1
CHANNEL 3
CHANNEL 5
CHANNEL 15
DRAM BANK1

FIG_5

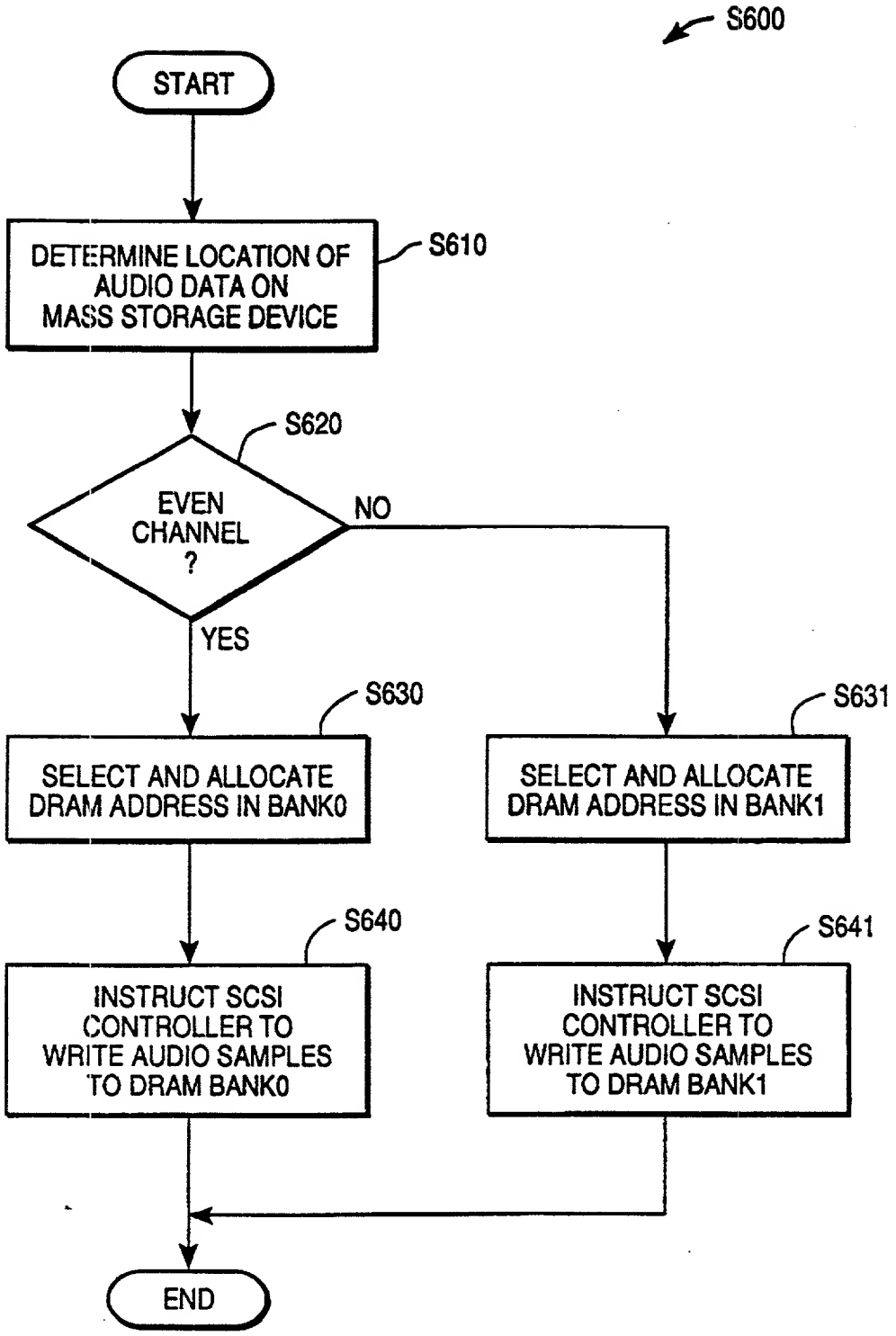
S600
START
DETERMINE LOCATION OF AUDIO DATA ON MASS STORAGE DEVICE
S610
S620
EVEN CHANNEL ?
NO
YES
S630
SELECT AND ALLOCATE DRAM ADDRESS IN BANK0
S631
SELECT AND ALLOCATE DRAM ADDRESS IN BANK1
S640
INSTRUCT SCSI CONTROLLER TO WRITE AUDIO SAMPLES TO DRAM BANK0
S641
INSTRUCT SCSI CONTROLLER TO WRITE AUDIO SAMPLES TO DRAM BANK1
END

FIG_6